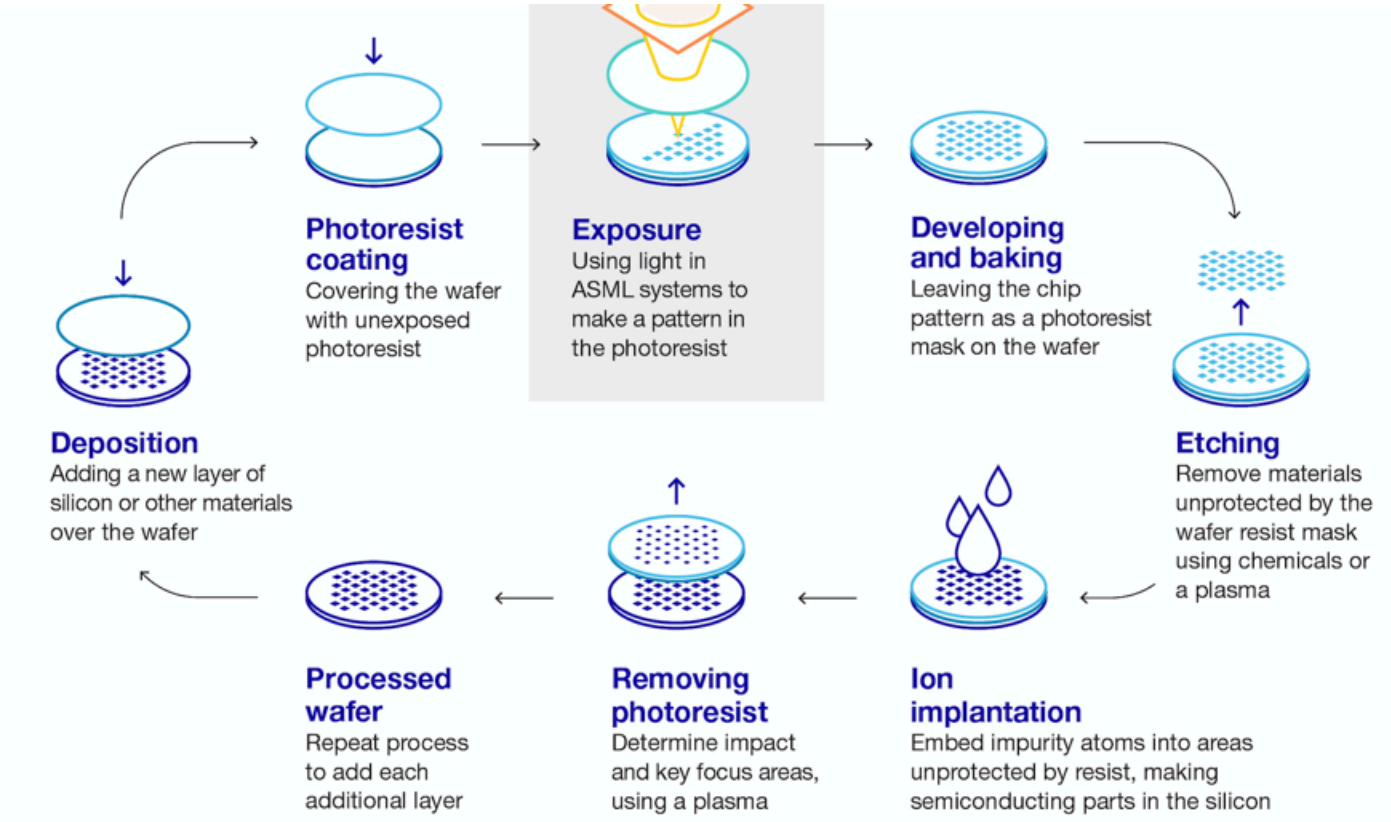
Semiconductor Fabrication Overview - Top Mark Capital

It all starts with a clean wafer

A wafer (also called a slice or substrate) is a thin slice of semiconductor, such as a crystalline silicon (c-Si), used for the fabrication of integrated circuits and, in photovoltaics, to manufacture solar cells. The wafer serves as the substrate for microelectronic devices built in and upon the wafer. It undergoes many microfabrication processes along the way to final packaging as an integrated circuit (figure 1).[5]

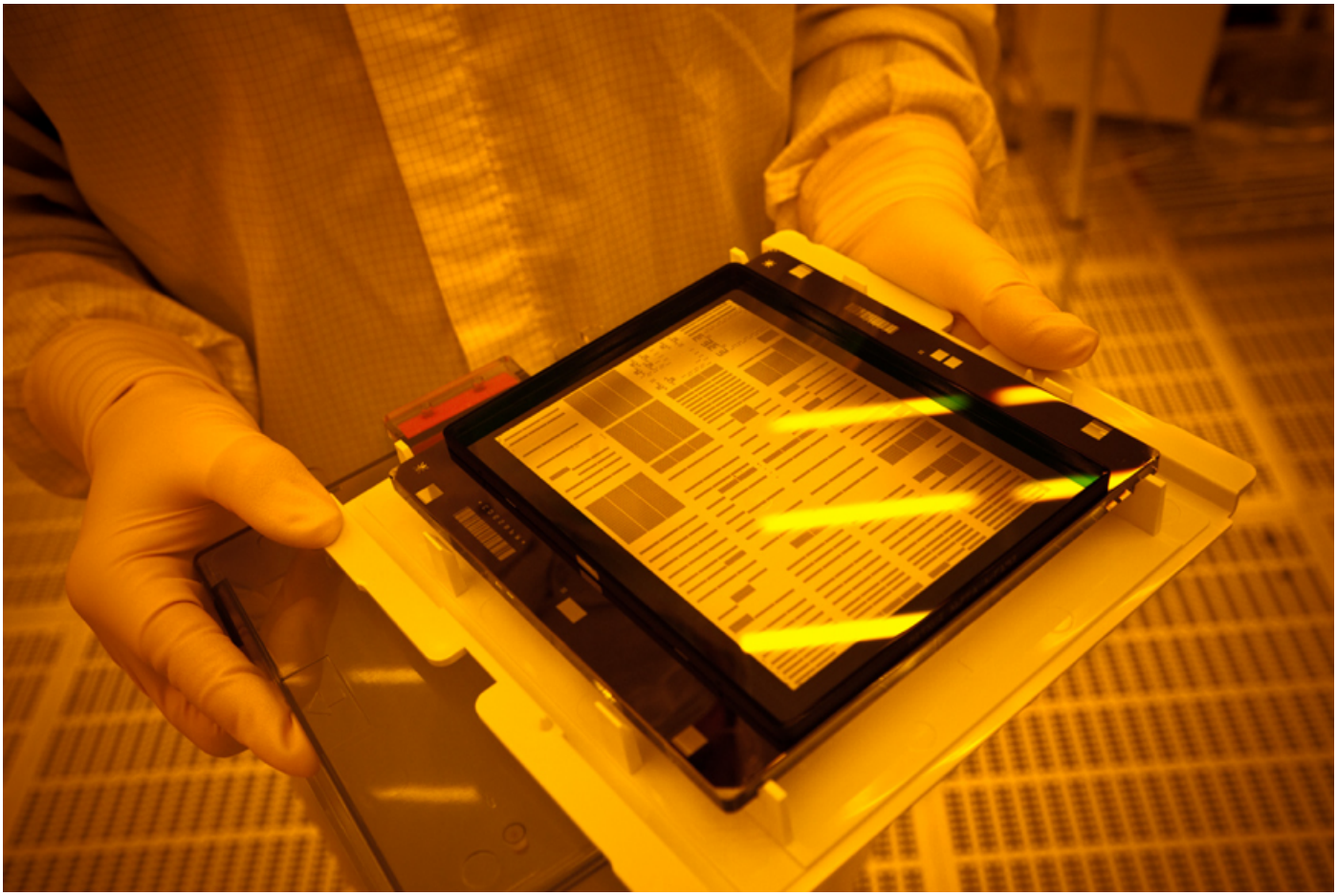


As wafer widths shrink, semiconductor purity has become an important issue. Fabrication plants are pressurized with filtered air to remove even the smallest particles, which could come to rest on the wafers and contribute to defects. To prevent oxidation and to increase yield, FOUPs and semiconductor capital equipment may have a hermetically sealed pure

nitrogen environment with ISO class 1 level of dust[4-1].

Modern semiconductor fabrication follows the following approximate process:

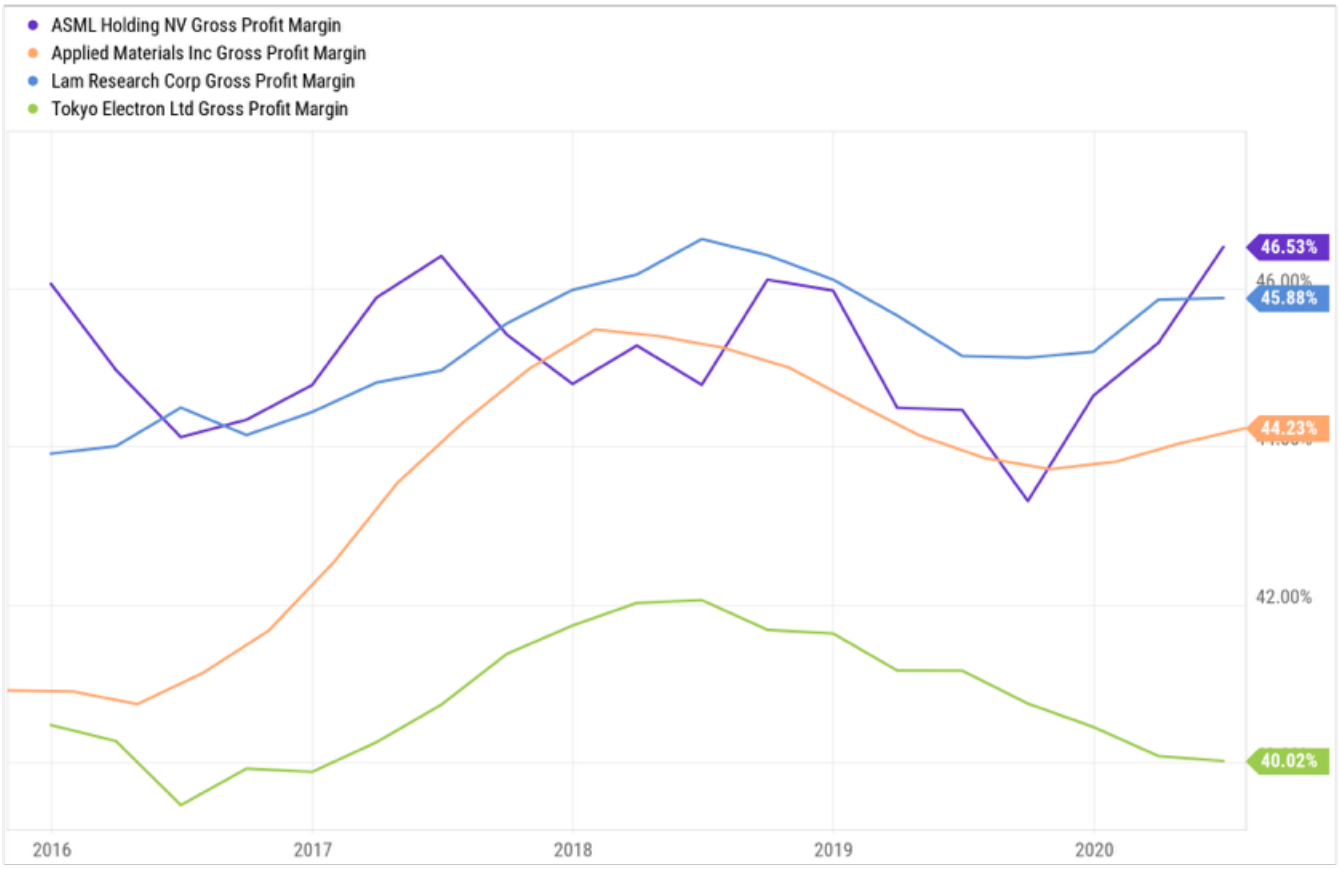
1. *Deposition* adds a new layer of silicon or other material over the wafer. Relevant companies include: Applied Materials, Tokyo Electron Ltd, Lam Research. Different types of coatings are applied using different methods, some of these include...
    1. Chemical Vapor Deposition (CVD) - CVD is used to deposit dielectric and metal films on a wafer
    2. Physical Vapor Deposition (PVD) - PVD is used to deposit high quality metal films.
    3. Epitaxy - Epitaxy (or epi) is a technique for growing silicon (e.g. silicon with another element) as a uniform crystalline structure on a wafer to form high quality material for the device circuity.
    4. *Photoresist coating* covers the wafer with unexposed photoresist.
2. *Exposure* uses light to make patterns in the photoresist. This is generally referred to as **lithography**. This is the heart of chipmaking. Comparable to silkscreening, instead of ink, light is shone through a glass photomask (figure 2) onto a silicon substrate coated with photoresist. The light weakens the photoresist, leaving a pattern on the surface of the silicon. Later processes etch trenches into and expose the substrate that is not covered by photoresist. ASML Holding NV is the leading company in the lithography space and is the sole supplier of EUV technology which is enabling the latest generation of geometric shrinking (5nm in production and 2nm on the horizon). Canon and Nikon also have lithography capabilities but their options are specialized to the imaging markets and are not used for logic nor memory chip production.



3. *Developing and Baking* solidifies the photoresist mask on the wafer.
4. *Etching* removes materials unprotected by the photoresist resist mask. Relevant companies include: Applied Materials Inc, Tokyo Electron Ltd, Lam Research.
    1. Etch - Etching is used many times throughout the IC manufacturing process to selectively remove material from the surface of a wafer.
    2. Selective Removal - Selective removal is a new etch technology intended to remove a material of a particular composition without damaging materials of different composition that coexist on the wafer.
5. *Ion Manipulation* embeds impurity atoms to make semiconducting parts. Applied Materials Inc.
6. *Removing Photoresist* readies the wafer for the next layer.
7. *Repeat* for each additional layer. This process can be repeated 100+ times[3-1].

There are many more processes and tools not covered here that are necessary to build logic and memory chips (cleaning of wafers and testing, for example), but the steps above capture the high level core processes being used today.

I've broken the semiconductor manufacturing equipment companies down into *lithography* and *everything else*. Companies in the *everything else* category include Applied Materials Inc, Tokyo Electron Ltd and Lam Research and many others. These companies have some overlapping and some specialized equipment. In the *lighography* category, on the other hand, ASML Holding NV appears to have a monopoly on the technologies, however, it does not appear to be able to command additional margin over the companies that supply *everything else* (Figure 3).



Furthermore, ASML Holding NV provided 2025 guidance of $15-25bn[3-2]. Marking, at best, a 66% increase in revenue (over 5 years), yet the company

trades at a price to sales ratio that is higher than the *everything else* peers (figure 4).

Finally, on a total return basis, ASML Holding NV has had lower returns than all of it's peers over the past 5 years (figure 5), though the returns have been quite good and nothing to scoff at.

ASML Holding NV acts as an integrator of technologies, and while it develops some technology in house, it also sources technology from many suppliers. As such, these vendors likely enjoy strong negotiating power which weighs on ASML's ability to generate extraordinary returns.

1. Super iPhone, The Clever, accessed 10/3/20↩
2. Moore's Law, Wikipedia, accessed 10/3/20↩
3. ASML 2019 Annual Report↩↩↩
4. Semiconductor device fabrication, Wikipedia, accessed 10/3/20↩↩
5. Wafer - electronics, Wikipedia, accessed 10/3/20↩